I claim:

1. A capacitor in an integrated semiconductor circuit, comprising:

a semiconductor substrate having a doped region formed therein;

a first electrode connected to said doped region;

a second electrode;

a capacitor dielectric insulating said first electrode from said second electrode; and

a barrier layer disposed below said capacitor dielectric, said barrier layer consisting essentially of a compound formed from a transition element and a material selected from the group consisting of phosphorus, sulfur, and arsenic.

2. The capacitor according to claim 1, wherein said first electrode is directly connected to said doped region.

3. The capacitor according to claim 1, which further comprises a connection structure connecting said first electrode to said doped region.

4. The capacitor according to claim 1, wherein said barrier layer is disposed directly underneath said capacitor dielectric and covers an entire interface between said first electrode and said capacitor dielectric.

5. The capacitor according to claim 3, wherein said barrier layer is disposed underneath said first electrode and covers an entire interface between said first electrode and said connection structure.

6. The capacitor according to claim 1, wherein said barrier layer is disposed underneath said first electrode and covers an entire interface between said first electrode and said doped region.

7. The capacitor according to claim 1, wherein said capacitor dielectric consists of a material selected from the group consisting of dielectric material and ferroelectric material, and has a value of □ > 100.

8. The capacitor according to claim 1, wherein said capacitor dielectric consists of a material selected from the group consisting of BST, SBT, PZT, and PLT.

9. The capacitor according to claim 1, wherein said first electrode consists of a material selected from the group

consisting of Pt-containing material, Ru-containing material, Rh-containing material, and Ir-containing material.

10. The capacitor according to claim 3, wherein said connection structure is made of a material selected from the group consisting of polysilicon and tungsten.

11. The capacitor according to claim 1, wherein said barrier layer is essentially a layer selected from the group consisting of a tungsten phosphide layer, a tantalum phosphide layer, and a hafnium phosphide layer.

12. A semiconductor configuration, comprising a capacitor according to claim 1, and an associated selection transistor which encompasses said doped region.

13. A method of producing a capacitor in an integrated semiconductor circuit, which comprises:

producing a first electrode on a semiconductor substrate and connecting, directly or via a connection structure, the first electrode to a doped region in the semiconductor substrate;

forming a barrier layer consisting essentially of a compound formed between a transition element and a material selected from the group consisting of phosphorus, sulfur, and arsenic,

and covering an entire exposed surface of the doped region or of the connection structure with the barrier layer;

producing a capacitor dielectric on the first electrode; and

producing a second electrode on the capacitor dielectric.

14. The method according to claim 13, wherein the barrier layer is produced by heat treatment in a pH_3 atmosphere on an electrode consisting of tungsten or on a connection structure consisting of tungsten.

15. The method according to claim 13, wherein the barrier layer is produced by CVD.

16. The method according to claim 13, wherein the barrier layer is applied surface-wide and is structured in an etching process with the use of the first electrode as a mask.

17. The method according to claim 13, wherein the capacitor dielectric consists of a material selected from the group consisting of dielectric material and ferroelectric material, and has a value of □ > 100.

18. The method according to claim 13, wherein the capacitor dielectric consists of a material selected from the group consisting of BST, SBT, PZT, and PLT.

19. A method of producing a capacitor in an integrated semiconductor circuit, which comprises:

producing a first electrode on a semiconductor substrate, the first electrode being connected directly or via a connection structure to a doped region in the semiconductor substrate;

producing a barrier layer on the first electrode, the barrier layer consisting essentially of a compound formed between a transition element and an element selected from the group consisting of phosphorus, sulfur, and arsenic, and covering an entire exposed surface of the first electrode;

producing a capacitor dielectric on the barrier layer; and

producing a second electrode on the capacitor dielectric.

20. The method according to claim 19, wherein the barrier layer is produced by heat treatment in a pH_3 atmosphere on an electrode consisting of tungsten or on a connection structure consisting of tungsten.

21. The method according to claim 19, wherein the barrier layer is produced by CVD.

22. The method according to claim 19, wherein the barrier layer is applied surface-wide and is structured in an etching process with the use of the first electrode as a mask.

23. The method according to claim 19, wherein the capacitor dielectric consists of a material selected from the group consisting of dielectric material and ferroelectric material, and has a value of □ > 100.

24. The method according to claim 19, wherein the capacitor dielectric consists of a material selected from the group consisting of BST, SBT, PZT, and PLT.